CLAIMS

[0052] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a memory device, said method comprising:

forming at least a portion of a capacitor structure for a memory cell within a memory array area of said memory device;

heat treating said capacitor structure; and

forming metal plugs down to active areas of said substrate after heat treating said capacitor structure, wherein at least a portion of said metal plugs formed down to said active areas are for both N-channel and P-channel peripheral logic transistors of a semiconductor substrate located outside said memory array area containing said memory cell.

2. A method of forming a memory device, said method comprising:

forming a lower electrode layer of a memory cell capacitor;

forming a dielectric layer in contact with said lower electrode layer;

heat treating said lower electrode and dielectric layer;

after said heat treating operation, forming an upper electrode layer in contact with said dielectric layer; and

after forming said upper electrode layer, forming metal contacts contiguous to active areas of each of an N-channel and P-channel transistor in a peripheral logic area.

3. A method of fabricating metallized plugs in a memory device, said method comprising the steps of:

providing a substrate having a memory cell array area and a peripheral circuitry area, wherein each of said memory cell array area and said peripheral circuitry area comprise at least one transistor of a first conductivity type and said peripheral circuitry area further comprises at least one transistor of a second conductivity type; said at least one memory cell array area transistor being an access transistor for a memory cell;

further processing said memory cell array area, to form at least one capacitor which is associated with said access transistor;

applying heat to anneal said capacitor;

defining multiple plug openings in material layers over said substrate at said periphery circuitry area of said substrate, wherein at least one of said plug openings exposes an active area of said transistor having said first conductivity type and at least one of said plug openings exposes an active area of said transistor having said second conductivity type; and

forming a metal layer over said substrate and into said plug openings to contact said active areas after said heat is applied to said memory cell array area.

4. A method as in claim 3 wherein said first conductivity type is N+.

5. A method as in claim 4 wherein said second conductivity type is P+.

6. A method of forming a memory device, said method comprising:

forming a pair of spaced word lines;

forming source and drain regions on opposite sides of said word lines to define a plurality of memory cell access transistors within a memory cell array area;

forming a pair of access transistors sharing a source/drain region;

forming at least one first insulating layer over said access transistors;

forming a pair of capacitor polysilicon plugs and a bit line polysilicon plug through said first insulating layer to said source and drain regions of said access transistor;

forming at least one second insulating layer over said polysilicon plugs;

forming container capacitors, respectfully associated with one of said access transistors in said second insulating layer over and in electrical communication with respective capacitor polysilicon plugs;

heat treating said container capacitors;

forming N-channel and P-channel peripheral logic transistors outside said memory cell array area;

after said heat treating, forming metal plugs to contact each of said N-channel and P-channel peripheral logic transistors through said first and second insulating layer;

forming at least one third insulating layer over said container capacitors; and

forming metal contacts through said third insulating layer to contact said metal plugs.

7. A method of forming a memory device, said method comprising:

forming memory cell access transistors in a memory cell array area of said memory device;

forming N-channel and P-channel periphery logic transistors in a peripheral logic area of said memory device;

forming at least portions of capacitors associated with said access transistors in said memory cell array area;

heat treating said capacitor portions; and

after said heat treating, forming first metal conductors which contact with active areas of said N-channel and P-channel peripheral logic transistors.

8. A method as in claim 7 further comprising:

forming capacitor conductive plugs between said capacitors and a first active area of a respective access transistor and forming bit line conductive plugs to a second active area of said access transistors; and

forming second metal conductors to said bit line conductive plugs at the same time as said first metal conductors are formed.

9. A method as in claim 7 wherein said heat treating occurs after all portions of said capacitors are formed.

10. A method as in claim 7 wherein said first metal conductors have an oval top down cross-sectional shape.

11. A method as in claim 8 further comprising the step of forming upper metal plugs to contact said first metal conductors.

12. A method as in claim 11 further comprising the step of forming upper metal plugs to contact said bit line conductive plugs.

13. A method as in claim 11 wherein said upper metal plugs have a smaller diameter than said first metal conductors.

14. A method as in claim 12 wherein said upper metal plugs have a smaller diameter than respective ones of said bit line conductive plugs and said first metal conductors.

15. A method as in claim 13 wherein said first metal conductors have an oval top down cross-sectional shape.

16. A method as in claim 15 wherein said upper metal plugs have a round top down cross-sectional shape.

17. A method as in claim 8 further wherein said first conductors and said bit line conductive plugs are N-type plugs.

18. A method of forming a memory device, said method comprising:

forming a pair of spaced word lines;

forming source and drain regions on opposite sides of said word lines to define a plurality of memory cell access transistors within a memory cell array area;

forming a pair of access transistors sharing a source/drain region;

forming at least one first insulating layer over said access transistors;

forming a pair of capacitor polysilicon plugs and a bit line polysilicon plug through said first insulating layer to said source and drain regions of said access transistors;

forming at least one second insulating layer over said polysilicon plugs;

forming container capacitors, respectfully associated with each of said access transistors in said second insulating layer over and in electrical communication with respective capacitor polysilicon plugs;

heat treating said container capacitors;

forming N-channel and P-channel peripheral logic transistors outside said memory cell array area;

forming peripheral metal plugs through said second insulating layer to contact each of said N-channel and P-channel peripheral logic transistors after said heat treating;

forming at least one third insulating layer over said container capacitors;

forming a bit line contact through said second insulating layer to said bit line polysilicon plug after said heat treating; and

forming metal contacts through said third insulating layer to said peripheral metal plugs.

19. The method as in claim 18 wherein said bit line contact is formed of metal.

20. A method of forming a metallized contact to a periphery transistor, said method comprising:

providing a memory array area on a substrate for formation of first conductivity type transistors;

providing a peripheral array area on said substrate for formation of first and second conductivity type transistors;

forming first conductivity type transistors in said memory array area and in said peripheral array area wherein said first conductivity type transistors are associated with a first conductivity type active area;

forming second conductivity type transistors in said peripheral array area, wherein said second conductivity type transistors are associated with a second conductivity type active area;

providing a planarized first layer of an insulating material over said first and said second conductivity type transistors and over said first and second conductivity type active areas;

etching openings through said first insulating layer to expose active areas of said first conductivity type in said memory array area;

filling said openings with a conductive material having said first conductivity type to form at least three first conductivity type plugs, wherein at least

one of said first conductivity type plugs is a bit line plug and at least two of said first conductivity type plugs is a capacitor plug;

providing a planarized second layer of an insulating material over said first insulating layer and said bit line and capacitor plugs;

etching through said second insulating layer and portions of said capacitor plugs to form capacitor container openings;

forming capacitor structures in said capacitor container openings comprising the steps of: depositing a conductive layer within said capacitor container openings to form a bottom layer, planarizing an upper surface of said capacitor containers to remove any conductive layer material on said upper surface; depositing a dielectric layer over said substrate, depositing an upper capacitor plate over said dielectric layer;

annealing said capacitor structures by applying heat to at least one of said bottom layer, said dielectric layer, or said capacitor plate;

after annealing said capacitor structure, etching through said second insulating layer to define a bit line opening to expose a surface of said bit line plug and etching through said second insulating layer to define peripheral plug openings in said peripheral array area to expose active areas of said first and second conductivity type; and

depositing a metal layer over said substrate to form a metal plug in said memory array area to contact said surface of said bit line plug, and form metal plugs in said peripheral array area to contact active areas each of said first conductivity type and said second conductivity type.

21. A method of forming a metallized contact to a periphery transistor, said method comprising:

providing a memory array area on a substrate for formation of first conductivity type transistors;

providing a peripheral array area on said substrate for formation of first and second conductivity type transistors;

forming first conductivity type transistors in said memory array area and said peripheral array area wherein said first conductivity type transistors are associated with a first conductivity type active area;

forming second conductivity type transistors in said peripheral array area, wherein said second conductivity type transistors are associated with a second conductivity type active area;

providing a planarized first layer of an insulating material over said first and said second conductivity type transistors and over said first and second conductivity type active areas;

etching openings through said first insulating layer to expose active areas of said first conductivity type in said memory array area;

filling said openings with a conductive material having said first conductivity type to form at least three first conductivity type plugs, wherein at least one of said first conductivity type plugs is a bit line plug and at least two of said first conductivity type plugs is a capacitor plug;

providing a planarized second layer of an insulating material over said first insulating layer and said first conductivity type plugs;

etching through said second insulating layer and portions of said capacitor plugs to form capacitor container openings;

forming capacitor structures in said capacitor container openings comprising the steps of: depositing a conductive layer within said capacitor container openings to form a bottom layer, planarizing an upper surface of said capacitor containers to remove any conductive layer material on said upper surface; depositing a dielectric layer over said substrate, depositing an upper capacitor plate over said dielectric layer;

annealing said capacitor structures by applying heat to at least one of said bottom layer, said dielectric layer, or said capacitor plate;

after annealing said capacitor structure, etching through said second insulating layer to define peripheral plug openings in said peripheral array area to expose active areas of said first and second conductivity type; and

depositing a metal layer over said substrate to form metal plugs in said peripheral array area to contact respective active areas of said first conductivity type and said second conductivity type.

22. A method as in claim 21 further comprising the steps of:

planarizing said metal layer to expose said capacitor plate;

etching said capacitor plate and said dielectric layer away from said metal plugs and said bit line plug;

depositing a third layer of an insulating material over said substrate;

etching contact openings through said third insulating layer to expose said metal plugs in said peripheral array area;

etching contact openings through said second insulating layer and said third insulating layer to expose said bit line plug in said memory array area; and

depositing a conductive layer over said substrate so as to fill said contact openings and form conductive contacts to said metal plugs and said bit line plug.

23. A memory device comprising:

a memory array area and a peripheral circuitry area, said memory array area comprising at least one access transistor of a first conductivity type and at least one capacitor for storing a data value which is associated with said access transistor, said peripheral circuitry area comprising at least one transistor of a first conductivity type and at least one transistor of a second conductivity type, and at least one first metal plug electrically connected to an active area of said transistor of said first conductivity type and at least one second metal plug electrically connected to an active area of said transistor of said second conductivity type.

24. The memory device of claim 23 wherein said first and second metal plugs have an oval top down cross-sectional shape.

25. The memory device of claim 24 wherein said first conductivity type is N+.

26. The memory device of claim 25, wherein said second conductivity type is P+.

27. A memory device comprising:

a pair of spaced word lines;

source and drain regions on opposite sides of said word lines to define a plurality of memory cell access transistors within a memory cell array area;

a pair of access transistors sharing a source/drain region;

at least one first insulating layer formed over said access transistors;

a pair of capacitor polysilicon plugs and a bit line polysilicon plug formed through said first insulating layer to said source and drain regions of said access transistor;

at least one second insulating layer formed over said polysilicon plugs;

container capacitors, respectively associated with one of said access transistors in said second insulating layer over and in electrical communication with respective capacitor polysilicon plugs;

N-channel and P-channel peripheral logic transistors outside said memory cell array area wherein said N-channel and P-channel peripheral logic transistors comprise first metal plugs to contact said N-channel peripheral logic transistor and second metal plugs to contact said P-channel peripheral logic transistor, said first metal plugs and said second metal plugs being formed through said first and second insulating layers,

a first bit line contact formed through said second insulating layer to said bit line polysilicon plug;

at least one third insulating layer over said container capacitors; and

metal contacts formed through said third insulating layer to said first metal plugs, said second metal plugs, and said first bit line contact.

28. The device of claim 27 wherein said first and second metal plugs have an oval top down cross-sectional shape.

29. The device of claim 28 wherein said metal contacts have a round top down cross-sectional shape.

30. The device of claim 27 wherein said metal contacts have a smaller diameter than said first and second metal plugs.

31. The device of claim 30 wherein said first metal plugs and said bit line plugs are in an N-channel transistor area.

32. The device of claim 27, wherein said bit line contact and said respective metal contact formed through said insulating layer are a unitary structure.

33. A memory device comprising:

a memory array area comprising transistors of a first conductivity type, wherein said first conductivity type transistors are associated with a first conductivity type active area;

a peripheral array area comprising transistors of said first conductivity type and further comprising transistors of a second conductivity type wherein said second conductivity type transistors are associated with a second conductivity type active area;

a first insulating layer formed over said memory array area and said peripheral array area;

a pair of capacitor plugs and a bit line plug formed through said first insulating layer in said memory array to contact said first conductivity type active area;

a second insulating layer formed over said first insulating layer, said capacitor plugs and said bit line plug;

capacitor containers formed in at least said second insulating layer and in contact with said capacitor plugs;

a metal plug in said memory array area formed through said second insulating layer to contact said bit line plug,

metal plugs in said peripheral array area formed through said first and second insulating layer to respective contact active areas of said first conductivity type and said second conductivity type.

34. A memory device comprising:

a memory array area comprising transistors of a first conductivity type, wherein said first conductivity type transistors are associated with a first conductivity type active area;

a peripheral array area comprising transistors of said first conductivity type and further comprising transistors of a second conductivity type wherein said second conductivity type transistors are associated with a second conductivity type active area;

a first insulating layer formed over said memory array area and said peripheral array area;

a pair of capacitor plugs and a bit line plug formed through said first insulating layer in said memory array to contact said first conductivity type active area;

a second insulating layer formed over said first insulating layer, said capacitor plugs, and said bit line plug;

capacitor containers comprising a bottom plate, a dielectric layer and an upper capacitor plate formed in at least said second insulating layer;

metal plugs in said peripheral array area formed through said first and second insulating layer to respective contact active areas of said first conductivity type and said second conductivity type;

a third insulating layer formed over said capacitor containers, said metal plugs, and said second insulating layer;

a metal bit line contact formed through said second and third insulating layer to contact said bit line plug; and

metal contacts formed through said third insulating layer to contact said metal plugs in said peripheral array area.

35. The device of claim 34 wherein said metal plugs have an oval top down cross-sectional shape.

36. The device of claim 35 wherein said metal contacts have a round top down cross-sectional shape.

37. The device of claim 34 wherein said metal contacts have a smaller diameter than said first and second metal plugs.

38. The device of claim 37 wherein said first conductivity type is N+.